R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

The present invention concerns an apparatus comprising an array of memory cells, a refresh circuit, a first monitor cell, a second monitor cell, and a control circuit. The refresh circuit may be configured to refresh the array of memory cells in response to a refresh control signal. The first monitor cell may be configured to have a charge leakage similar to the memory cells. The second monitor cell may be configured to have a discharge leakage similar to the memory cells. The control circuit may be configured to generate the refresh control signal in response to either a voltage level of the first monitor cell rising above a first pre-determined threshold level or a voltage level of the second monitor cell dropping below a second pre-determined threshold level, where the first and second threshold levels are different.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1, 2 and 4-20 under 35 U.S.C. §102(b) as being anticipated by Tatematsu '369 (hereinafter Tatematsu) is respectfully traversed and should be withdrawn.

Tatematsu is directed to a self-refresh semiconductor memory device responsive to a refresh request signal (Title).

In contrast, the present invention (claim 1) provides (i) an array of memory cells, (ii) a refresh circuit configured to refresh the array of memory cells in response to a refresh control signal, (iii) a first monitor cell configured to have a charge leakage similar to the memory cells, (iv) a second monitor cell configured to have a discharge leakage similar to the memory cells, and (v) a control circuit configured to generate the refresh control signal in response to either a voltage level of the first monitor cell rising above a first pre-determined threshold level or a voltage level of the second monitor cell dropping below a second pre-determined threshold level, where the first and second threshold levels are different. Claims 12 and 13 include similar recitations. Tatematsu does not disclose or suggest each and every element of the presently claimed invention, arranged as in the present claims. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Specifically, assuming, *arguendo*, (i) the pseudo memory cell PMC1 of Tatematsu is similar to the presently claimed first monitor cell, (ii) the pseudo memory cell PCM2 of Tatematsu is similar to the presently claimed second monitor cell and (iii) the sense cell array 14 and leak detector 16 of Tatematsu are similar to the presently claimed control circuit (as suggested in the last eight lines on page 2 of the Office Action and for which

Applicant's representative does not necessarily agree), Tatematsu fails to disclose each and every element of the presently claimed invention. In particular, Tatematsu does not disclose or suggest either (i) **a first monitor cell configured to have a charge leakage similar to the memory cells** or (ii) a control circuit configured to generate the refresh control signal in response to either **a voltage level of the first monitor cell rising above a first pre-determined threshold level** or a voltage level of the second monitor cell dropping below a second pre-determined threshold level, where the first and second threshold levels are different, as presently claimed.

Tatematsu states that the capacitors of the pseudo memory cells PCM1 and PCM2 are charged to Vcc each time a refresh occurs (see FIG. 1, column 3, line 45 through column 4, line 3 and column 5, lines 39-45 of Tatematsu). Tatematsu further states that:

> When the potential of at least one of the capacitors in the pseudo cells falls below a predetermined level, the refresh request signal is generated . . . . (Abstract of Tatematsu).

Tatematsu describes the operation of the pseudo memory cells as follows:

> Initially, assume that a charge leakage occurs in one of the capacitors of the pseudo memory cells PMC1, PMC2, ---, e.g., capacitor C1 of the cell PMC1. In this state, when the potential Vcx of the capacitor C1 falls below the aforementioned predetermined level (Vcx <Vcc -VTHN -VTHP), the corresponding transistor Q1 is turned ON, so that the signal ϕs on the line L2 is raised from low level to high level. At this time, the signal ϕk is

> still high level, and therefore, the refresh request signal ϕRFSH becomes high level for a short time.
>
> When the refresh request signal ϕRFSH is high level, each transistor of the pseudo memory cells PMC1, PMC2, PMC3, ---, is turned ON, and thus each capacitor C1, C2, C3, ---, is charged to the Vcc level. Accordingly, each capacitor voltage Vcx is raised to the Vcc level, and thus all of the capacitors, including the leaking capacitor, are "refreshed". (column 5, lines 24-45 of Tatematsu).

Thus, the capacitors in the pseudo memory cells of Tatematsu are always charged during refresh to the Vcc level and the refresh request signal is only generated when the potential on the capacitors of the pseudo memory cells fall below a predetermined level. Furthermore, Tatematsu is silent regarding either (i) a charge leakage resulting in an increase in the potential Vcx of the capacitors in the pseudo memory cells PCM1, PCM2, etc. or (ii) generating the refresh request signal in response the potential Vcx of any of the pseudo memory cells rising above a predetermined level.

Because (i) the pseudo memory cells of Tatematsu are always charged to the Vcc level, (ii) the refresh request signal of Tatematsu is generated only when the potential of the capacitor of the pseudo memory cell falls below a predetermined level, (iii) Tatematsu is silent regarding the potential of the capacitors of the pseudo memory cells rising in response to charge leakage and (iv) Tatematsu is silent regarding generating the refresh request signal when the potential of the capacitor of the pseudo memory

cell rises above a second predetermined level, Tatematsu does not disclose or suggest either (i) **a first monitor cell configured to have a charge leakage similar to the memory cells**, as presently claimed, or (ii) a control circuit configured to generate the refresh control signal in response to either **a voltage level of the first monitor cell rising above a first pre-determined threshold level** or a voltage level of the second monitor cell dropping below a second pre-determined threshold level, where the first and second threshold levels are different, as presently claimed. Therefore, Tatematsu does not disclose or suggest each and every element of the presently claimed invention, arranged as in the present claims. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Claims 1-11 and 14-20 depend, either directly or indirectly, from claims 1 or 13 which are believed to be allowable. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claim 3 under 35 U.S.C. §103(a) as being unpatentable over Tatematsu is respectfully traversed and should be withdrawn.

Claim 3 depends indirectly from claim 1 which is believed to be allowable. Furthermore, the Office's use of a portion of the

present specification as the basis for the obviousness rejection is improper. Specifically, The conclusory statement that "it would have been an obvious matter of design choice for one having ordinary skill in the art at the time the invention was made to include a on-shot circuit in the apparatus as [stated] by the applicant (see specification, page 9, line 1-8)" does not adequately address the issue of motivation to modify or combine. In particular, "it is improper, in determining whether a person of ordinary skill would have been led to [a] combination of references, simply to '[use] that which the inventor taught against its teacher.'" (*In re Lee*, 61 USPQ2d 1430, 1434 (Fed. Cir. 2002) citing *W.L. Gore v. Garlock, Inc.*). Therefore, the Office Action fails to meet the Office's burden of factually establishing a *prima facie* case of obviousness (MPEP §2142). As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

As such, the presently claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our office Account No. 50-0541.

Respectfully submitted,

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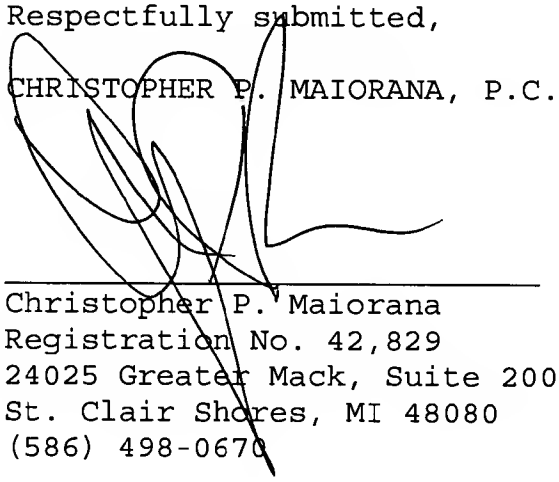

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